IN THE SPECIFICATION

1. Please amend the paragraph starting on page 12, line 2 of the application as follows:

To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide improved bundle alignment and dispersal circuitry for use in a data processor. According to an advantageous embodiment of the present invention, the data processor includes execution clusters, an instruction cache, an instruction issue unit, and alignment and dispersal circuitry. Each execution cluster includes an instruction execution pipeline having a number of processing stages, and each execution pipeline is a number of lanes wide. The processing stages execute instruction bundles, where each instruction bundle has one or more syllables. Each lane is capable of receiving one of the syllables of an instruction bundle. The instruction cache includes a number of cache lines. The instruction issue unit receives fetched cache lines and issues complete instruction bundles toward the execution clusters. The alignment and dispersal circuitry receives the complete instruction bundles from the instruction issue unit and routes each received complete instruction bundle to a correct one of the execution clusters. The complete instruction bundles are routed as a function of at least one address bit associated with each complete instruction bundle. ~~comprises: 1) C execution clusters, each of the C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each the instruction execution pipelines is L lanes wide, each of the L lanes capable of receiving one of~~

~~the one-to-S syllables of the instruction bundles; 2) an instruction cache capable of storing a plurality of cache lines, each of the cache lines comprising C*L syllables; 3) an instruction issue unit capable of receiving fetched ones of the plurality of cache lines and issuing complete instruction bundles toward the C execution clusters; and 4) alignment and dispersal circuitry capable of receiving the complete instruction bundles from the instruction issue unit and routing each the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one address bit associated with each of the complete instruction bundles.~~

2. Please amend the paragraph starting on page 13, line 17 of the application as follows:

According to yet another embodiment of the present invention, the alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each received complete instruction bundle to any one of the [[C]] execution clusters.

3. Please amend the paragraph starting on page 14, line 9 of the application as follows:

In one embodiment of the present invention, [[L=4]] each execution pipeline is four lanes wide.

4. Please amend the paragraph starting on page 14, line 10 of the application as follows:

In another embodiment of the present invention, [[C=3]] the data processor includes three execution clusters.